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TOWNSEND and TOWNSEND and CREW LLP

By: Lynne Carrier Cass

PATENT
Docket No.: 000939-073311US
Client Ref. No.: P01HA010/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Hong Koo Kim

Application No.: 09/747,779

Filed: December 22, 2000

For: FABRICATION METHOD AND STRUCTURE FOR FERROELECTRIC NONVOLATILE MEMORY FIELD EFFECT TRANSISTOR

Examiner: Marcos D. Pizarro Crespo

Art Unit: 2814

DECLARATION OF HONG KOO KIM UNDER 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Professor HONG KOO KIM, declare:

1. I am a U.S. citizen, residing at 1611 Country Club Drive, Pittsburgh, PA 15237, and am a professor in Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, Pennsylvania, and have been a faculty member of the University of Pittsburgh since 1990 (assistant professor from 1990 to 1996, associate professor from 1996 to 2002, and full professor since 2002).

2. I attended Seoul National University in Korea from 1977 to 1981 and received a Bachelor of Science degree in Electronics Engineering, and Korea Advanced Institute of Science and Technology from 1981 to 1983 and a Master of

Science degree in Electrical Engineering, and Carnegie Mellon University in Pennsylvania from 1986 to 1989 and a Philosophy of Doctor degree in Electrical and Computer Engineering.

3. Since 2002, I have been Co-Director of the Institute of NanoScience and Engineering at the University of Pittsburgh. Since 1996, I have been Chair of the Western Pennsylvania Chapter of the American Vacuum Society. I have been a member of IEEE, Materials Research Society, and American Physical Society.

4. From 1983 to 1986, I had been a research staff at the Electronics and Telecommunications Research Institute in Korea.

5. I published over 50 refereed papers in the area of microelectronics, optoelectronics and nanophotonics, including the following papers on the ferroelectric nonvolatile memory devices: 1) "Ferroelectric nonvolatile memory field-effect transistors based on a novel buffer layer structure", Hong Koo Kim and Nasir Abdul Basit, International Journal of High Speed Electronics and Systems, vol.10, 39-46, 2000 (Invited Paper), 2) "Growth of highly oriented Pb(Zr,Ti)O3 films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field-effect transistors", Nasir Abdul Basit and Hong Koo Kim, Applied Physics Letters, vol.73, 3941-3943, 1998, and 3) "Lead-zirconate-titanate-based metal/ferroelectric/insulator/semiconductor structure for nonvolatile memories", Mingjiao Liu, Hong Koo Kim, and Jean Blacherc, Journal of Applied Physics, vol.91, 5985-5996, 2002.

6. I am an inventor of the above-identified U.S. Patent Application No 09/747,779, filed on December 22, 2000, which claims priority to Provisional U.S. Patent Application No. 60/173,1999, filed on December 27, 1999. This application relates to ferroelectric nonvolatile memory field effect transistors. I have read and understood this patent application and the claims now pending therein.

7. Embodiments of the present invention solved a major problem in developing a ferroelectric field-effect transistor (FEFET) structure for nonvolatile memory device applications. The well-known problem in this field has been on

integrating a ferroelectric layer on a silicon FET structure without sacrificing/compromising the characteristics of each part, i.e., an FET and a ferroelectric layer. Direct deposition of a ferroelectric layer on silicon surface usually results in poor interface properties (due to reaction or interdiffusion between the two materials during film deposition or post-deposition annealing processes). This has detrimental effects on the FET channel and the ferroelectric layer. Deposition of ferroelectric material on amorphous surface (i.e., oxidized silicon surface) usually results in an amorphous phase of the material which is either nonferroelectric or very weakly ferroelectric. Any attempt to grow oriented films that show ferroelectric property usually results in intermixing between ferroelectric and oxidized silicon due to the high temperature process involved. In prior work, a buffer layer of certain insulating materials (such as CeO2, CaF2 or SrTiO3) has been introduced between silicon and ferroelectric in order to alleviate this problem. Being directly deposited on crystalline surface of silicon, these buffer layers are usually grown highly oriented and are used as a template to deposit an oriented ferroelectric layer. While this structure shows improved interface properties compared with the ferroelectric/silicon structure, it still suffers from the problems of poor retention, carrier injection, and large leakage current.

In one embodiment we overcome this problem by employing the following materials system, layer structure and process steps: 1) Grow first a thin layer of amorphous silicon oxide on silicon surface using a standard thermal oxidation process in dry oxygen ambient. This oxidation process, commonly used in standard CMOS processes, is well known to provide the best quality of silicon surface passivation and thus the best properties of FET channels. 2) Grow an oriented buffer layer (MgO) on top of the thermally grown amorphous silicon oxide. This inventor has discovered that MgO can be grown highly oriented on amorphous silicon-oxide surface under certain process conditions. 3) Grow an oriented ferroelectric layer (for example, PZT) on top of the MgO buffer using the buffer layer as a template. The MgO is also found to well serve as a diffusion barrier between PZT and oxidized silicon.

8. I have read and understood the rejection in the final Office Action mailed on February 25, 2003. I have also read and understood the cited art in the final Office Action, including Hirai et al. (U.S. Patent No. 5,955,755), Kirin et al.(U.S. Patent No. 5,225,561), and Maiti et al. (U.S. Patent No. 6,020,024), that the Examiner has used to reject claims 1, 3-10, and 14-22. I have also reviewed the Amendment Under 37 C.F.R. § 1.116 mailed on April 25, 2003 and the Advisory Action mailed on May 20, 2003 by the Examiner in response to the Amendment Under C.F.R. § 1.116.

9. I have reviewed the Preliminary Amendment filed with the present Request for Continued Examination and the pending claims therein. The pending claims have been amended to clarify that

First, a silicon oxide layer is formed on silicon surface using a thermal oxidation process without any prior deposited material on the silicon surface. As well known by those skilled in the art, forming a silicon oxide layer directly on the silicon surface provides high-quality passivation of silicon surface, thereby providing enhanced FET channel characteristics.

Second, an oriented, insulating buffer layer (MgO) is formed on an amorphous silicon-oxide layer, rather than on silicon surface that has a crystalline structure. This process is based on our findings that a certain insulating material (such as MgO) can be grown self-oriented on amorphous surface (such as silicon oxide) under certain process conditions and thus can be used as a template to grow oriented ferroelectric layers (such as PZT).

Overall this embodiment is clearly different from that of Hirai et al. in which an oriented buffer layer is first formed on crystalline silicon surface and then a silicon oxide layer is formed sandwiched in between the silicon and insulating buffer by thermal annealing them in oxygen ambient. A silicon oxide resulting from the Hirai process is generally of lower quality than the silicon oxide formed directly on the silicon surface. The fact that Hirai discloses formation and use of the lower quality silicon oxide indicates to me that its inventors did not know how to form an oriented buffer layer on a

non-crystalline surface. The claims now pending in this application are clearly patentable over Hirai, Kirin, and Maiti.

10. Although the overall layer structure of the FEFET device discussed in this embodiment (metal/ferroelectric/insulating-buffer/silicon-oxide/silicon) has certain similarity to that of Hirai, the processes used in forming a silicon oxide buffer is very different in the two processes. Accordingly, the properties of the resulting silicon/silicon-oxide interface are expected to be different. In Hirai's method, an insulating buffer layer is grown directly on a crystalline silicon surface in order to obtain an oriented buffer layer. A silicon oxide layer is then formed by annealing the buffer-layer-covering the silicon surface in oxygen ambient. As such, the nature of Hirai' s silicon surface passivation cannot be the same as that of this embodiment, which employs a thermal oxidation on free silicon surface without any prior deposited material thereon.

11. Hirai, Kirin, and Maiti, alone or in combination, fail to disclose or suggest the claimed method of fabricating the non-volatile memory. Without providing any supporting information, Hirai et al. claimed that an alternative process sequence may be performed to implement the metal/ferroelectric/insulating-buffer/silicon-oxide/silicon structure, i.e., first form a silicon oxide layer and then an insulating buffer and a ferroelectric layer (U.S. Patent No. 5,955,755 column 7 line 66 to column 8 line 9). It is generally believed in this field that insulating materials usually do not grow self-oriented on amorphous surface. There is no suggestion in Hirai that they are aware of that MgO (or any other insulating buffer layer listed in their patent) has a tendency to grow self-oriented on amorphous surface. There is no disclosure in Hirai that they utilize this special property in their invention. Hirai describes six fabrication methods. All of them disclose forming an oriented buffer layer directly on crystalline silicon and then performing thermal annealing for silicon oxide formation. No explicit statement or supporting information is given about the possibility and utilization of forming a self-oriented buffer layer on amorphous surface.

12. The nature of the thermal annealing steps employed for the insulating buffer layers is also different for the two processes. In the present

embodiment, the purpose of this annealing step is to enhance the crystalline property of the deposited layer, i.e., to make it a highly oriented buffer layer grown on an amorphous surface. The MgO buffer layer is found to grow highly oriented on silicon oxide surface under the deposition and post-deposition annealing conditions disclosed in this embodiment. In the Hirai et al., the deposited buffer layer is grown oriented due to the template role played by the crystalline silicon surface. The purpose of their annealing step is then to form a silicon oxide layer at the interface between the buffer layer and silicon. In this annealing process of Hirai, oxygen is expected to diffuse through the buffer layer and to reach the silicon interface.

13. Considering the different conditions of silicon surface passivation (The silicon surface in Hirai is already covered/interfaced with an insulating buffer material, whereas the silicon surface in this invention is crystalline, free from any deposited material.), the resulting silicon interface properties (surface/interface states, etc.) are expected to be different between the two cases. Thermal oxidation of free silicon surface is the preferred way of passivating silicon surface in the standard CMOS processes due to resulting good FET channel properties. The FEFET devices thus fabricated show excellent performances in ferroelectric polarization switching and memory retention. (Please see the attached papers: Growth of highly oriented $PB(Zr,Ti)O_3$ films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field-effect transistors," Applied Physics Letter, Vol. 73, No. 26; and "Lead-zirconate-titanate-based metal/ferroelectric/insulator/semiconductor structure for nonvolatile memories," Journal of Applied Physics, Vol. 91, No. 9 .)

14. I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or nay patent issuing therefrom.

Date: July 24, 2003

Hong Koo Kim